**Lab 7: Introduction to Behavioral Verilog and Logic Synthesis**

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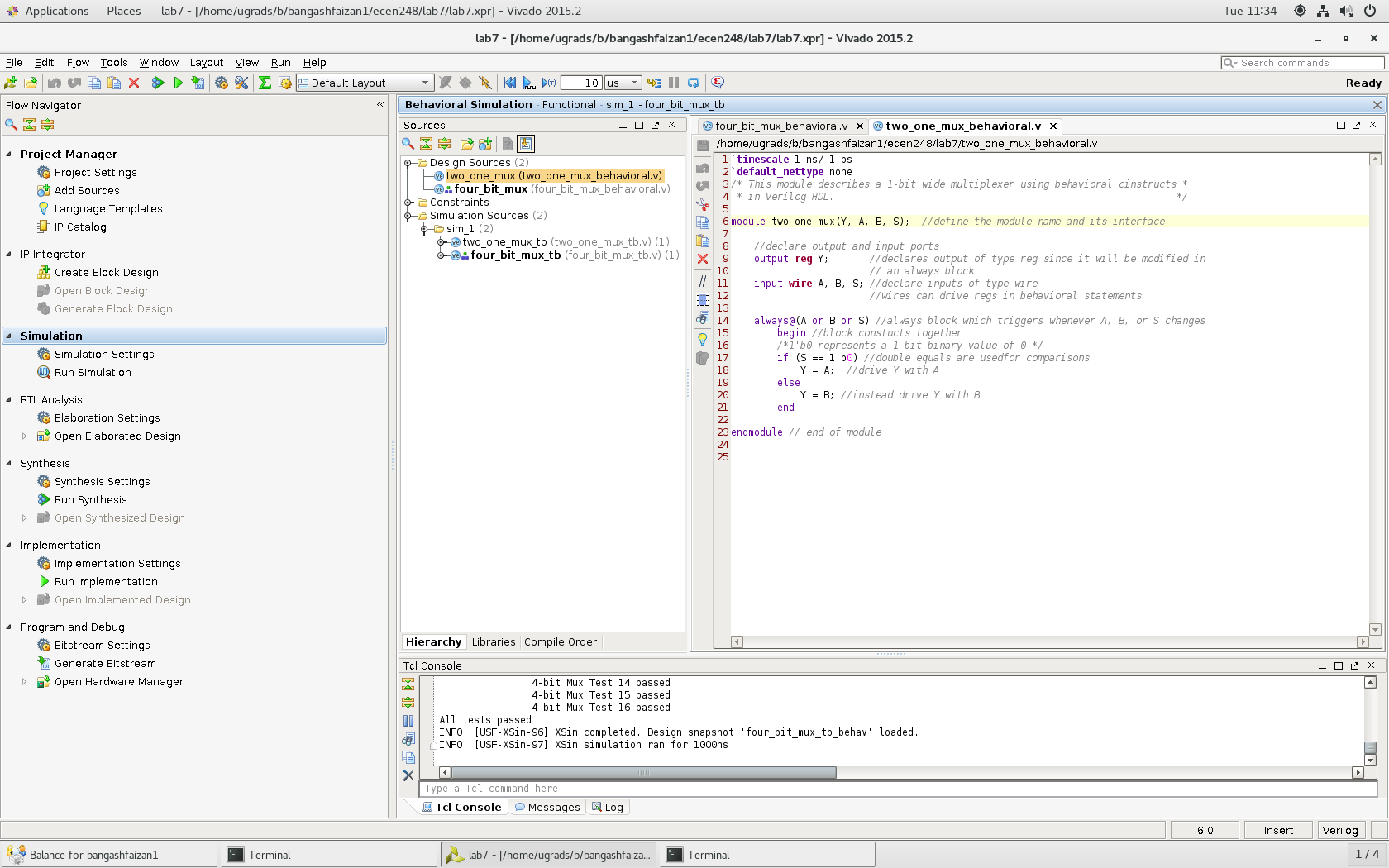
**Objectives** –

In this lab, we learned new ways to make verilog programs using behavioral modeling. This will allow us to do more with the program and not be so limited. With this, I can use **begin, end, initial,** and **always** keywords and allow for the outputs to change as the inputs change.

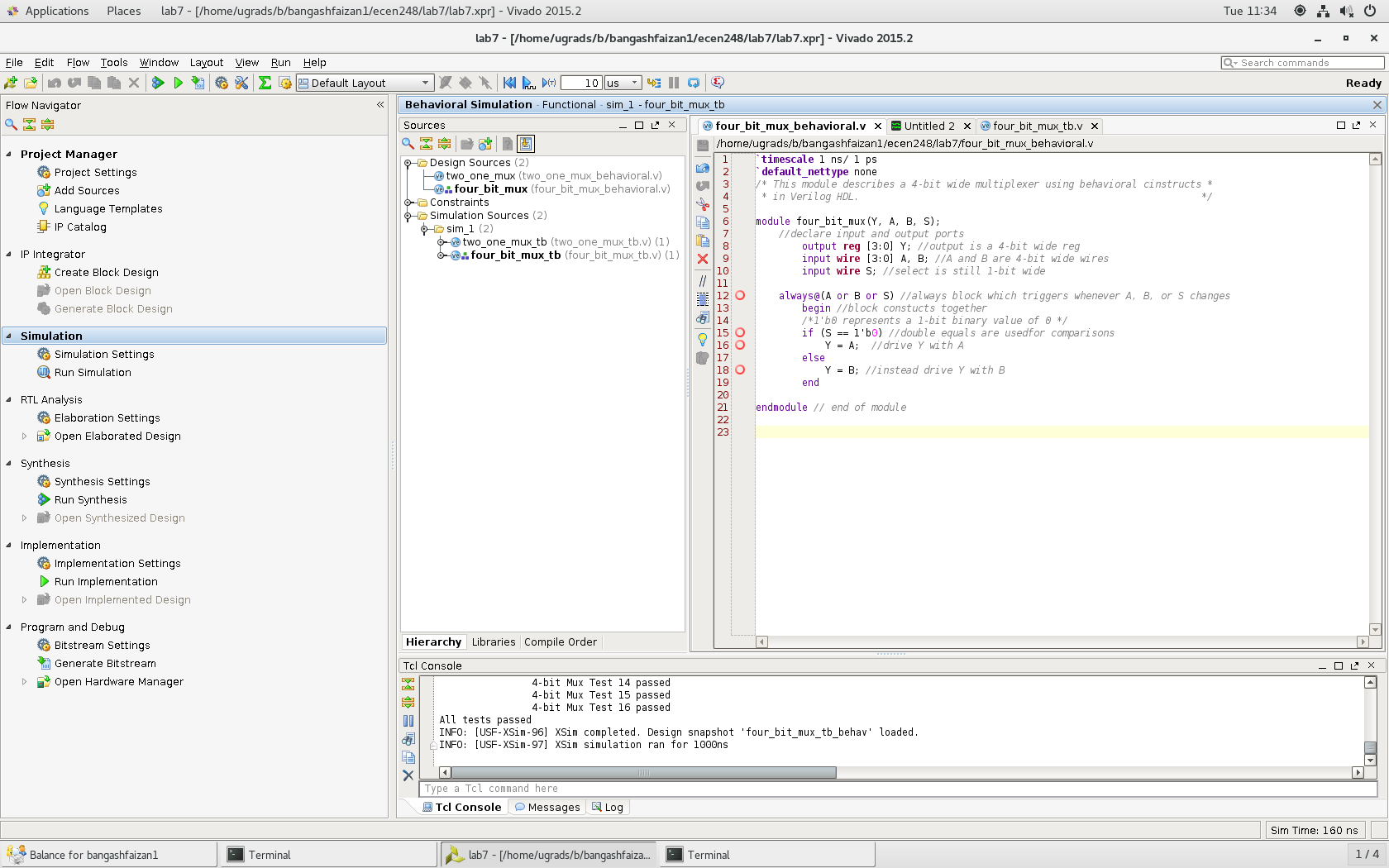
**Design** –

In this lab, we redesigned code from the past to allow it to be adapt to what was sent to it. Below is the code for each of the parts of the lab.

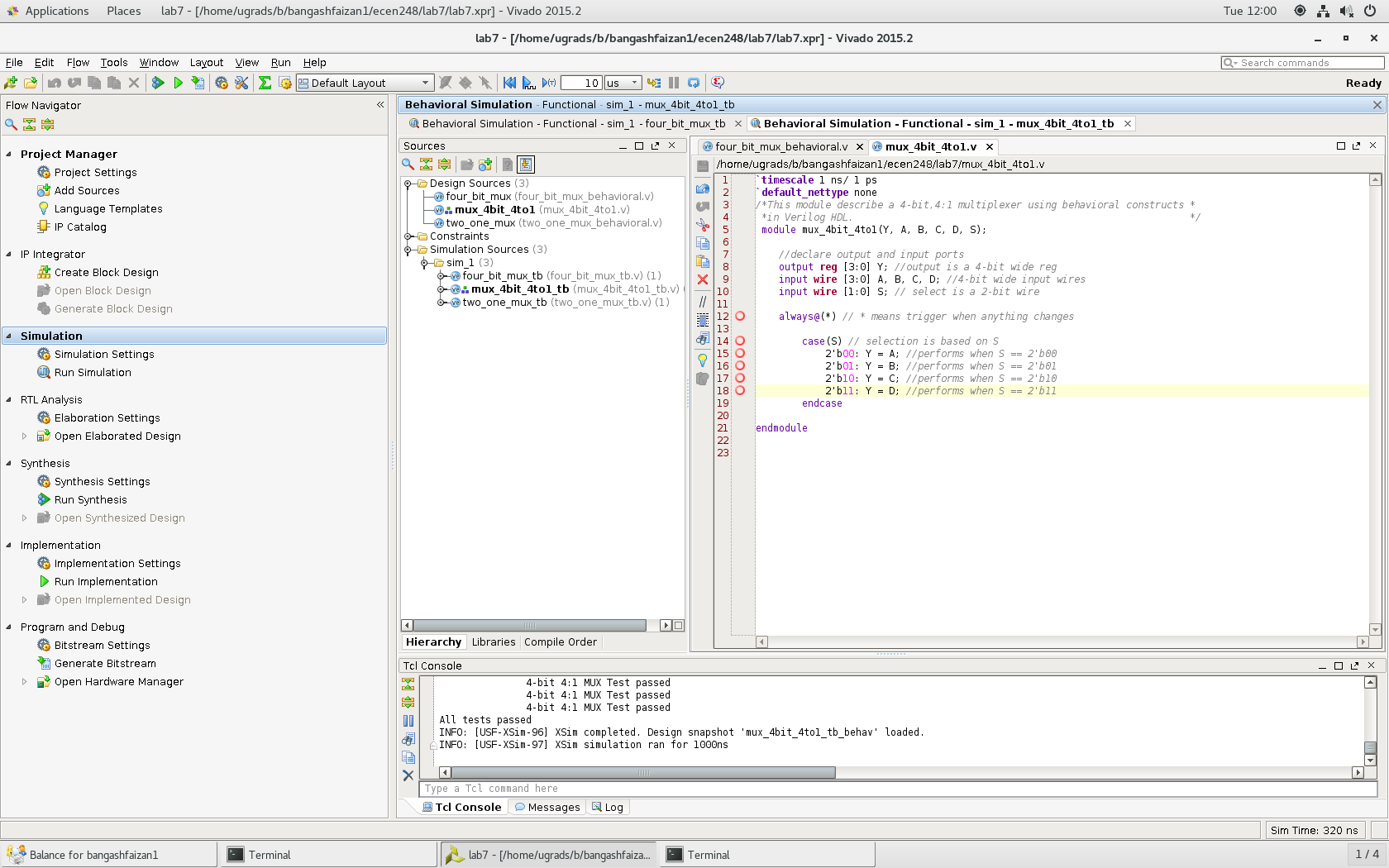
**1-Bit 2:1 MUX**



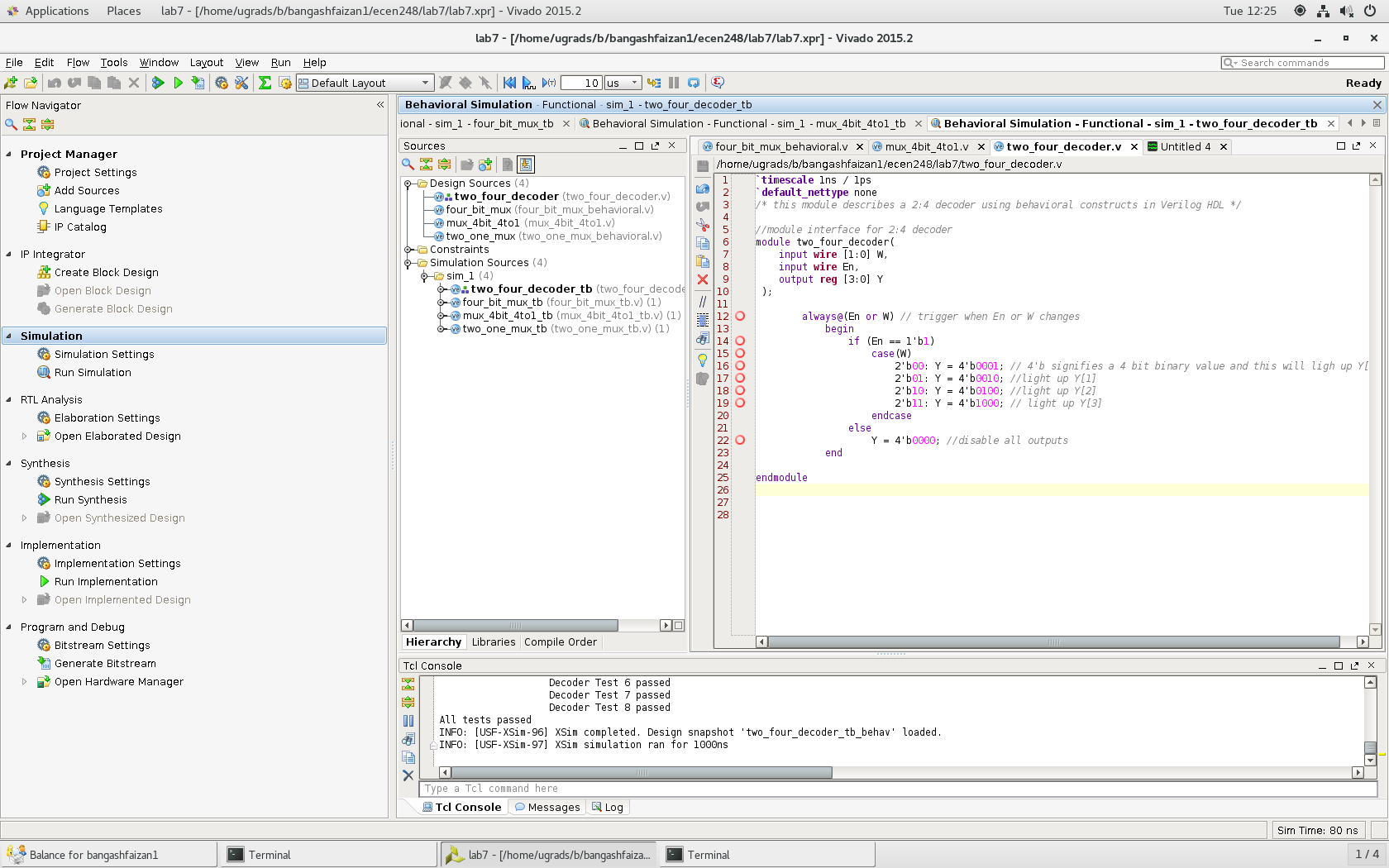
**4-Bit 2:1 Mux**



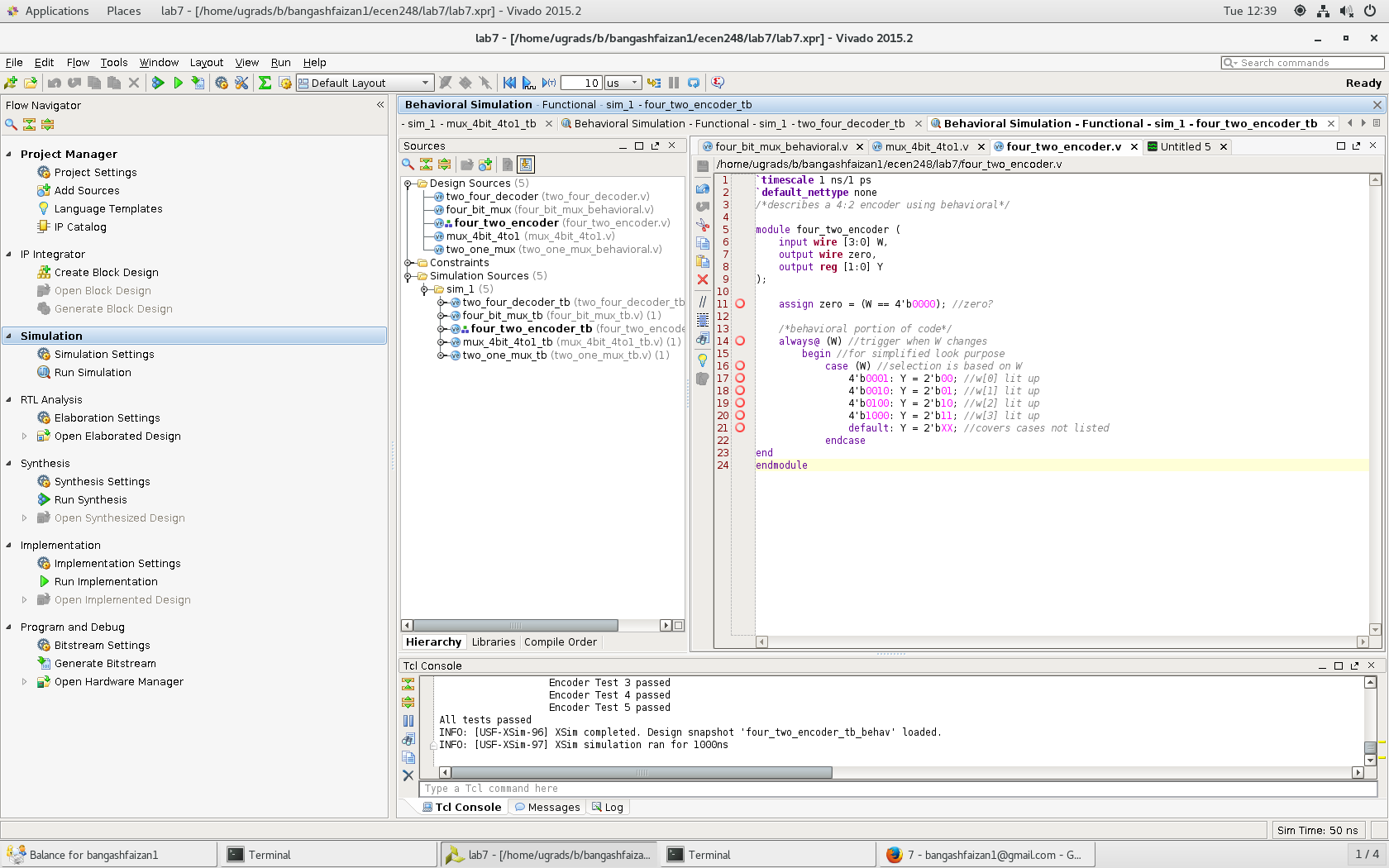
**4bit mux 4 to 1**

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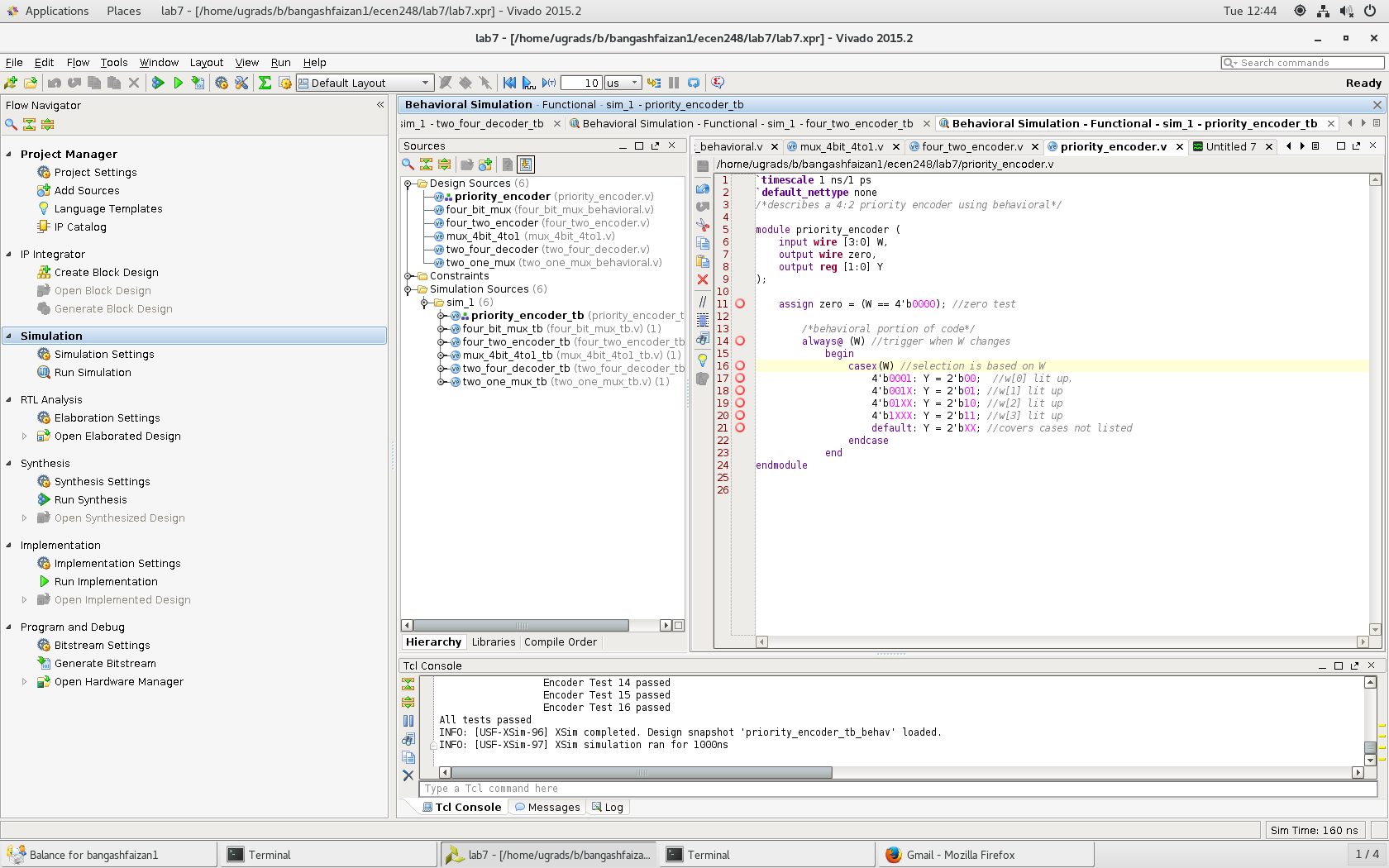
**2:4 Decoder**



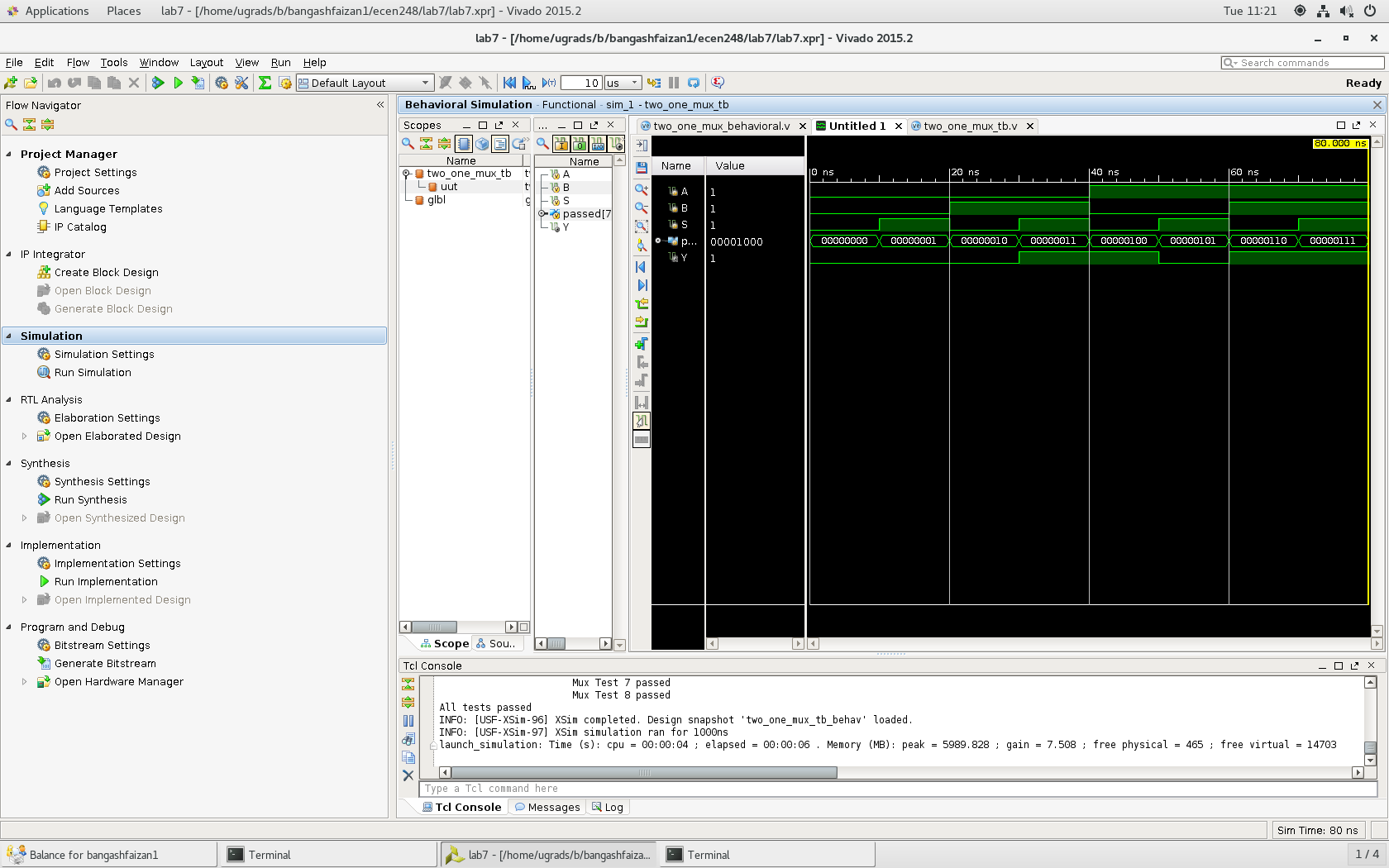
**4:2 Encoder**



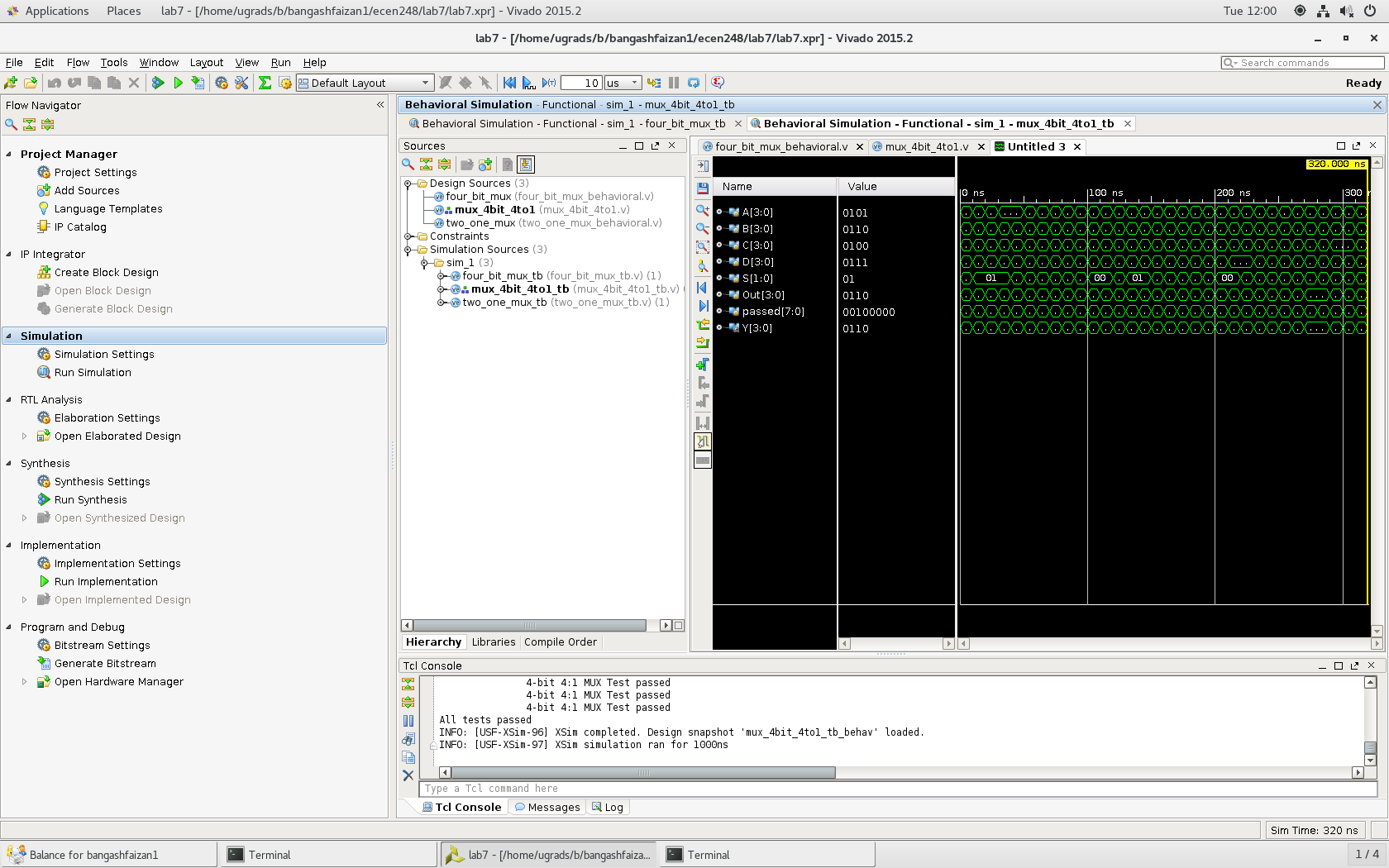
**4:2 Priority Encoder**



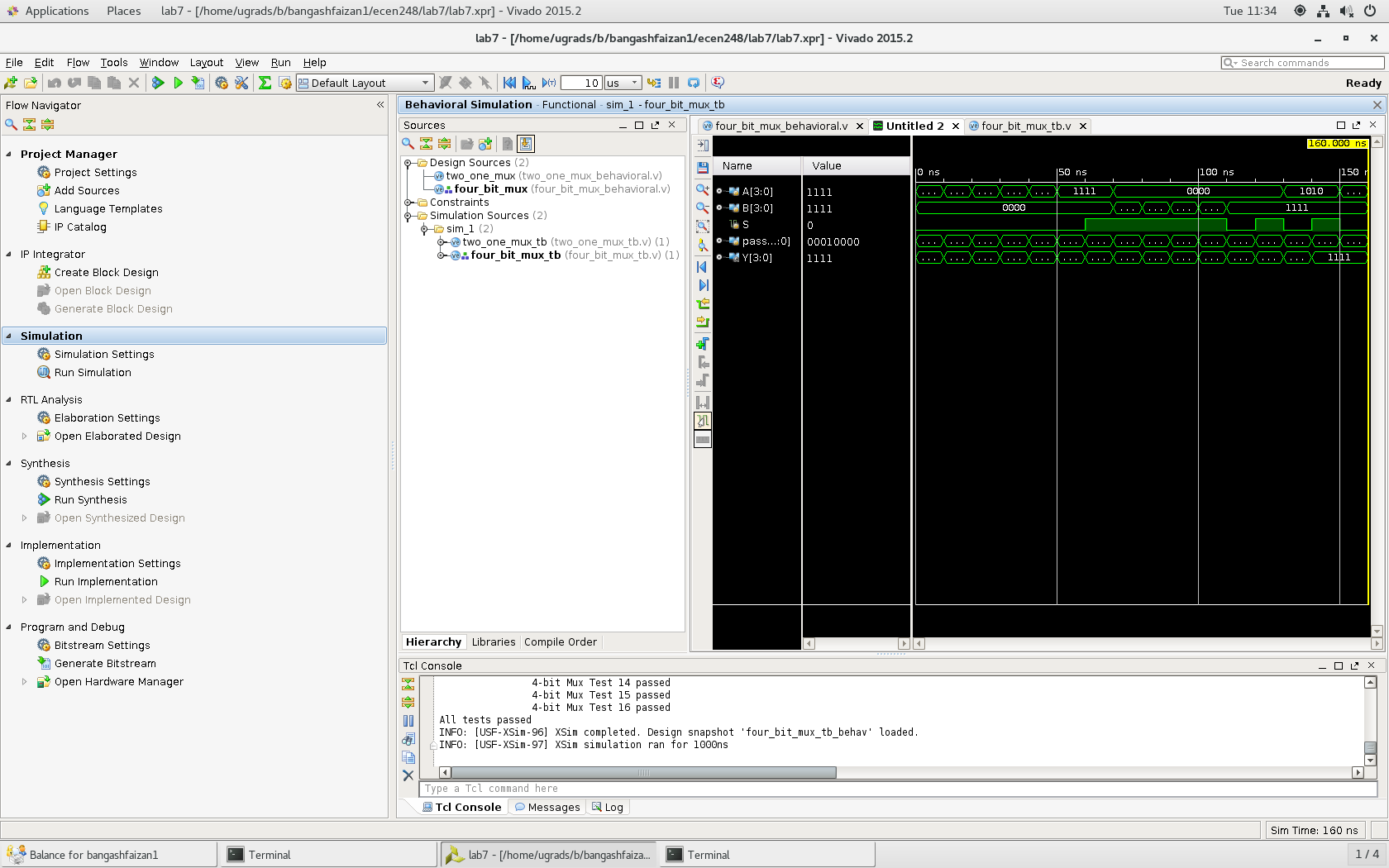
**Results:** Below are the waveform results for the lab.



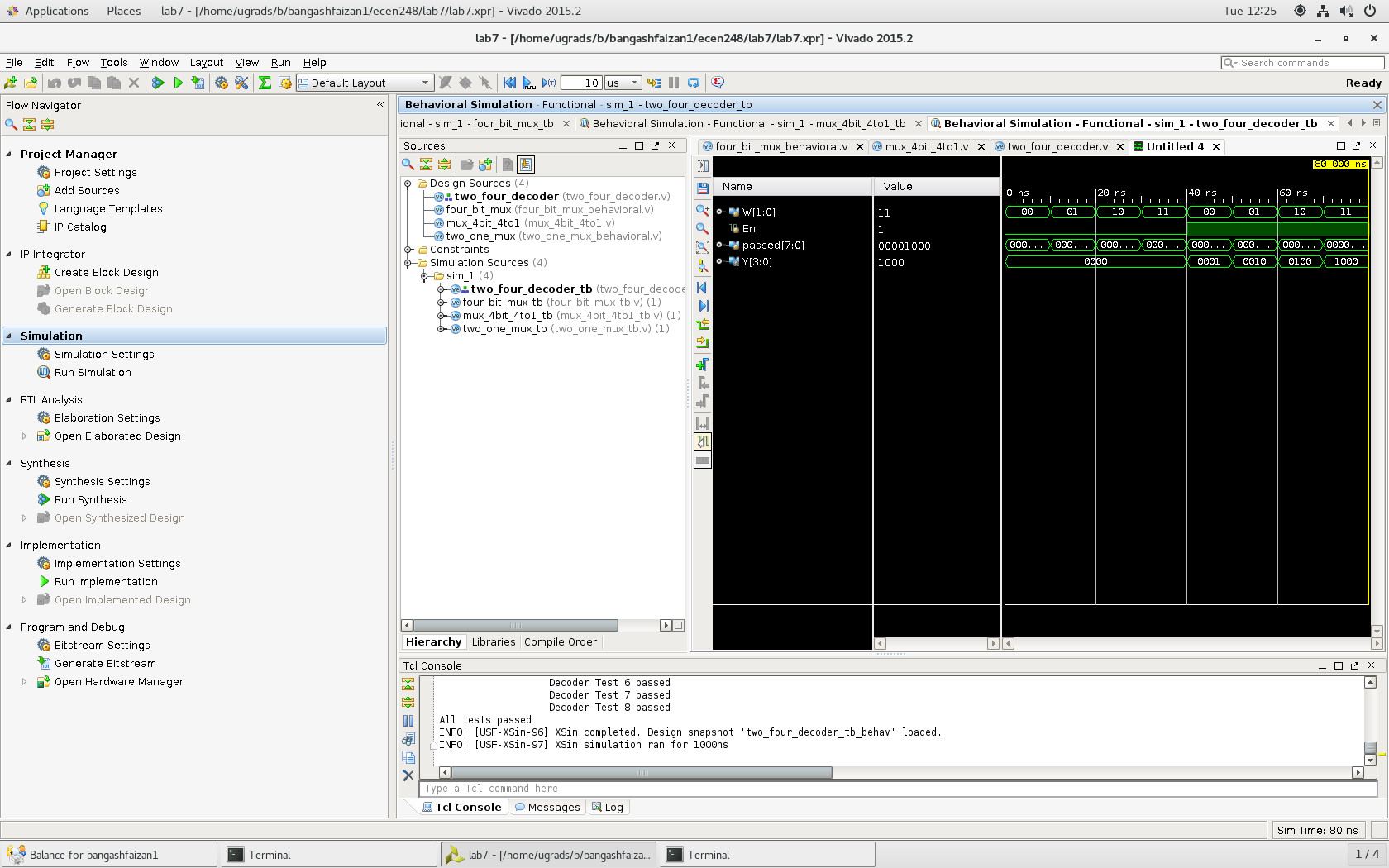
2:1 MUX Results



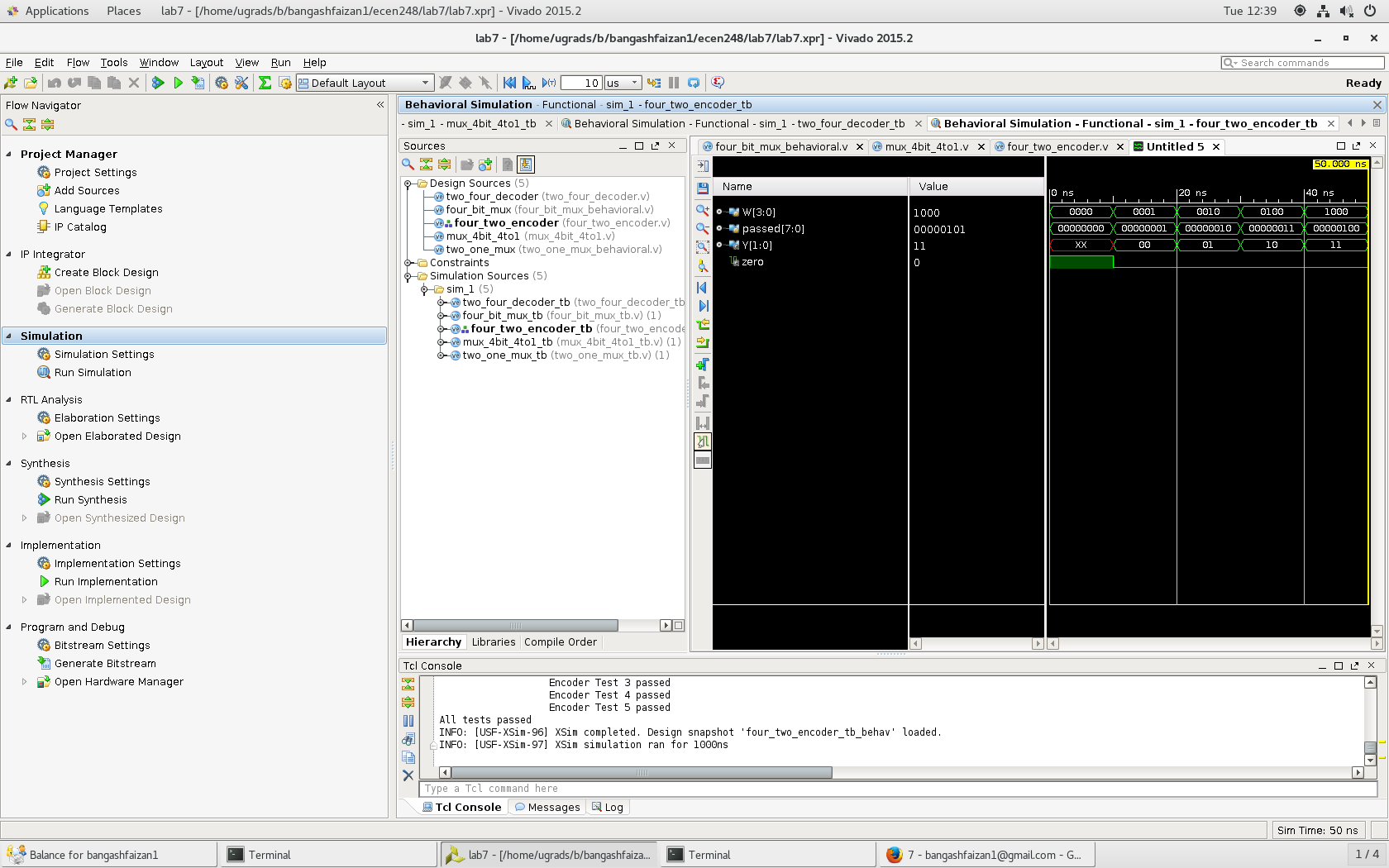
4:1 MUX results



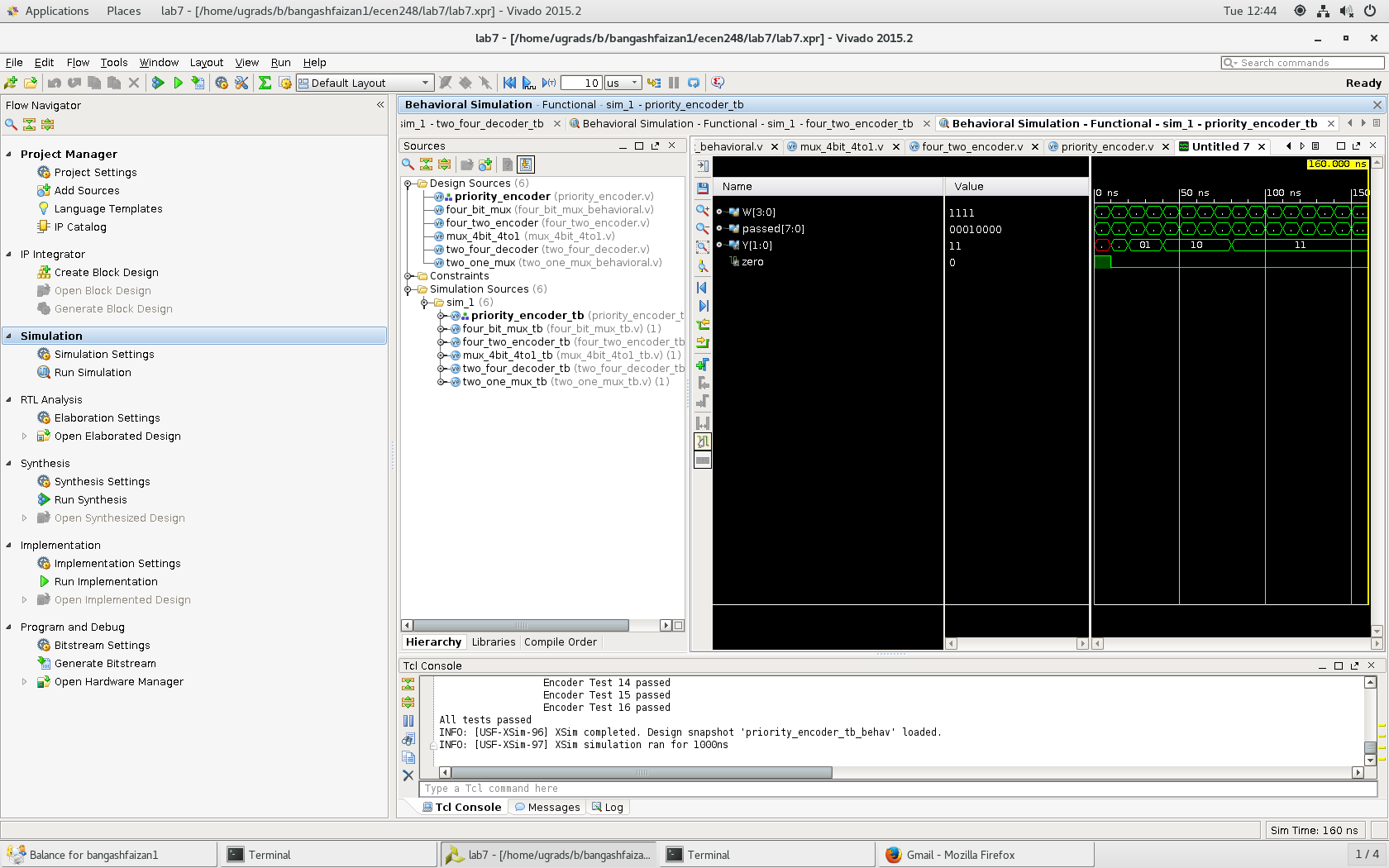
4:2 MUX behavioral



2:4 Decoder results



4:2 Encoder results



Priority encoder results

While mainly using behavioral verilog in this lab compared to structure and dataflow in last weeks lab, we can see a few advantages and disadvantages for each. An advantage of using structural instead of behavioral is that structural describes the structure of the gate schematic and can be easier to understand and fix if there are problems. However, a reason to use behavioral instead of structural is that behavioral takes advantage of the software and can be easier to implement.

The process of implementing a digital circuit on an FPGA is much more efficient and easier than a breadboard. Advantages of implementing circuits on an FPGA instead of a breadboard is that on the FPGA, you can implement larger circuits much easier than a breadboard. Also, it is much easier to find errors and debug a circuit through Verilog instead of a breadboard. Another huge advantage is that you don’t have to worry about failing hardware nearly as much. The disadvantage of using FPGA over a breadboard is that breadboards give hands on learning and provide more opportunities to understand why it works instead of just how.

**Conclusion –**

Overall, this lab was very helpful as it allowed me to learn how to use more types of verilog code as well as it gave me an intro into implementing the code onto the ZYBO board. This lab will be very helpful in the future as we start to work on more complex code and must implement our design in a timely manner. In this lab I ran into no issues and my code worked as expected other than a weird computer glitch where I was getting a syntax error for nothing. I had to fix the error by changing computers.